VertexCom

VC83X0

Product Brief

Version: 0.5

Release Date: Feb 25, 2019

General Description

VC83X0 (VC8300/VC8320) is a dual mode Power Line Communication (PLC) processor with integrated sub-GHz RF Transceiver. VC83X0 incorporates one 32-bit ARM Cortex M4 MCU, one 32-bit DSP, one embedded Flash memory, 6 UART interfaces, one SPI interface, one 10/100M Ethernet MAC, PLC MAC/PHY layer functions, Analog Front-End (AFE) and high current Line Driver.

VC83X0 supports multiple modern narrowband and broadband PLC standards for Smart Grid and other IIoT applications. In cooperation with the integrated high performance sub-GHz RF transceiver, VC83X0 delivers the optimum dual-mode (PLC + RF) hardware platform for AMI networking in Smart Grid connections. On top of VC83X0 Vertexcom's mesh software stack based on hop-by-hop PLC/RF transmission media selection provides the most effective solution to solve coverage and reliability difficulties encountered in a complicated outdoor environment.

Features

- 32-bit ARM Cortex M4 MCU
- Up to 6 UART interfaces
- One SPI interface (Master/Slave)
- 2 PWM
- One Ethernet MAC with RMII interface
- 2 MB embedded Flash memory
- 128 KB SRAM
- Support In-System Programming (ISP) of Flash memory via UART0 or SPI interface
- 3.3 V digital I/O
- Integrated DC/DC (3.3 V to 1.2 V) buck converter
- Package: QFN-88 (10 x 10mm)
- Operating temperature: -40 ~ +85 °C

PLC Processor Features

- Support multiple narrowband and broadband PLC Standards:
  - VC8300: G3-PLC, IEEE P1901.2, PRIME
  - VC8320: China SGCC Q/GDW 11612, IEEE 1901.1
- Frequency band:
  - VC8300: 0 - 500 KHz
  - VC8320: 1.9 MHz - 12.5 MHz

    SGCC HPLC 0.7 MHz - 2.99 MHz
- Integrated high linearity, high current and power efficient Line Driver to offer the lowest BOM cost for PLC applications
- Companion DC/DC buck converter VC6100 (Patented) for better power efficiency
- Modulation schemes: BPSK, QPSK, 8PSK and 16QAM
- Support HW AES-128/192/256 and SM2/SM3/SM4

Sub-GHz Transceiver Features

- Support IEEE 802.15.4g/Wi-SUN
- Support wireless M-Bus
- ISM Frequency bands: 315, 433, 490, 868, 915 MHz ISM
- Excellent selectivity performance
  - Adjacent channel rejection: 48 dB
  - Blocking performance: 75 dB
- Best-in-class receiver sensitivity
  - -109 dBm at 50 kbps GFSK
- Maximum data rate: 300 kbps
- Configurable maximum transmit output power
  - +20 dBm
  - +13 dBm
- Automatic output power ramping
- Current consumption
  - Shut-down: 70 nA
  - Sleep mode: 0.8 µA
  - Receive mode: 16 mA
  - Transmit mode: 96 mA at +20 dBm

- Modulation schemes: OOK, (G)FSK, 4(G)FSK and GMSK
- Automatic RX wake-up for low power listen
- Fast wake-up and AGC for low-power listen
- Functions for wireless link robustness
  - RF channel hopping
  - Retransmission
  - Auto-acknowledgement
- Digital RSSI and clear channel assessment for CSMA and listen-before-talk systems
- Support packet over packet reception for reliable communication
- Early termination of receive mode for incorrect preamble reception
- Hardware-based user identification listen to eliminate false wake-up

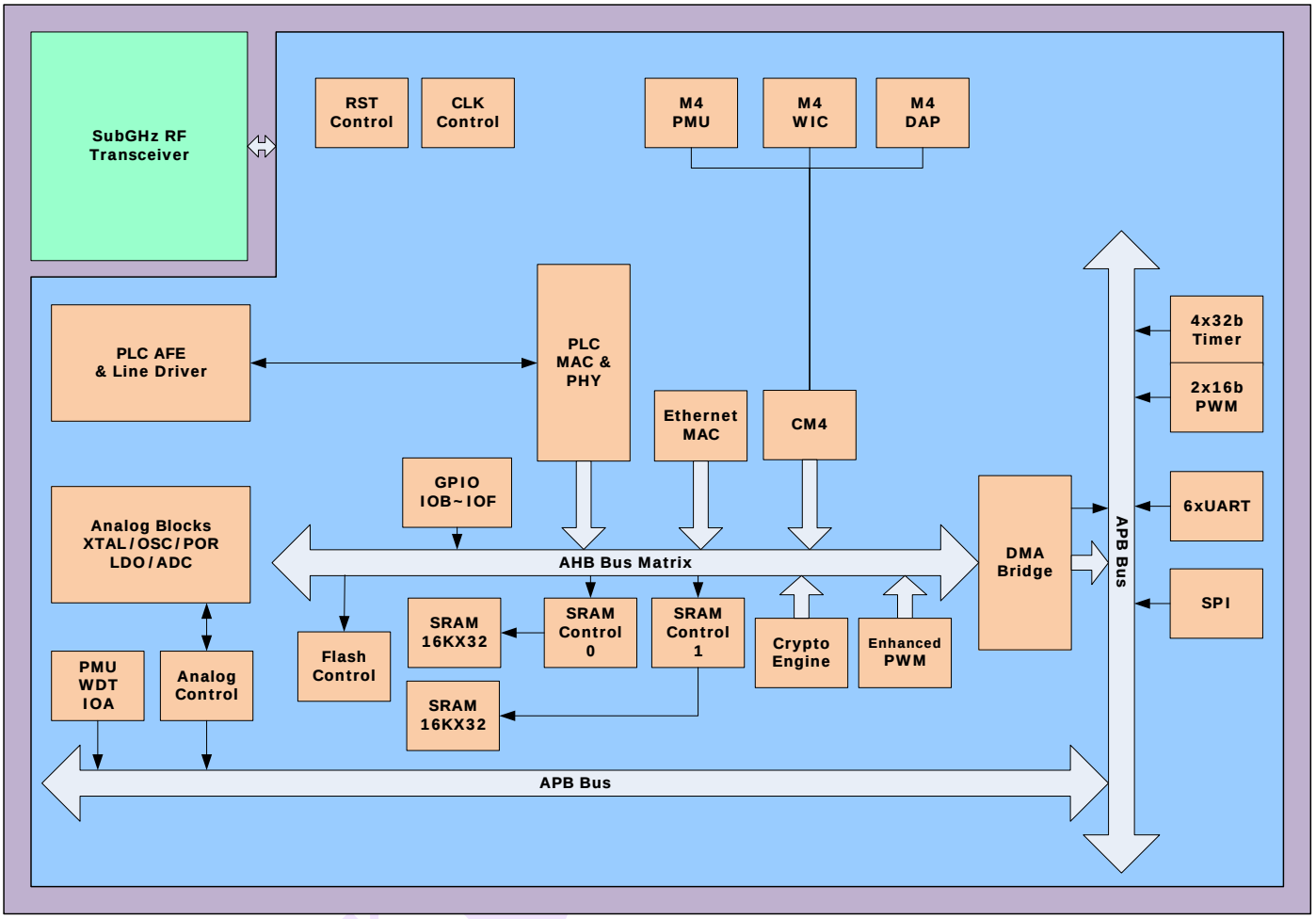
Dual-Mode Features

- Seamless integration of PLC and sub-GHz RF communication
- Best path selection mixing of wired and wireless channels
- L2 hybrid networking with common upper layers
  - Less memory overhead
  - Less delay through the path
  - Applicable to arbitrary upper-layer protocols
  - No modification effort for user applications
- Hop-by-hop selection of RF & PLC (RF-PLC-RF-PLC…)
  - Higher packet success rate than end-to-end approach (RF-RF-…-RF or PLC-PLC-…-PLC)
  - Interoperable with existing PLC nodes
  - Flexible to deploy (partial replacement is possible)
- Backbone for electricity/ gas/ heat/ water AMR

Applications

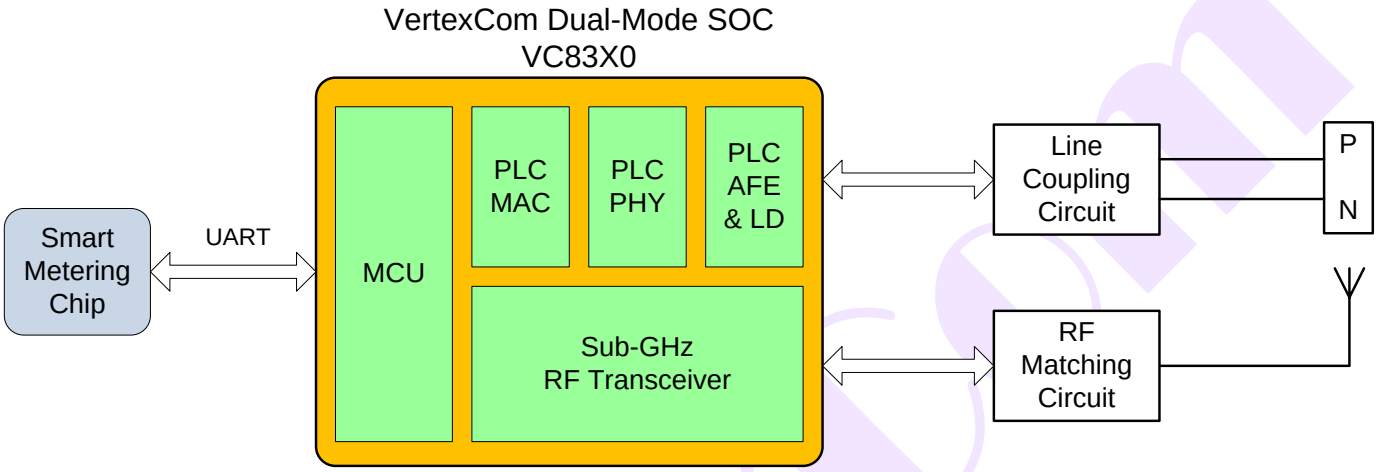
- Smart Grid communications
- Advanced Metering Infrastructure (AMI)
- Smart meters
- Power Line Communications data concentrators
- Street lighting automation
- Industrial monitoring and control
- Smart home and building

Functional Block Diagram

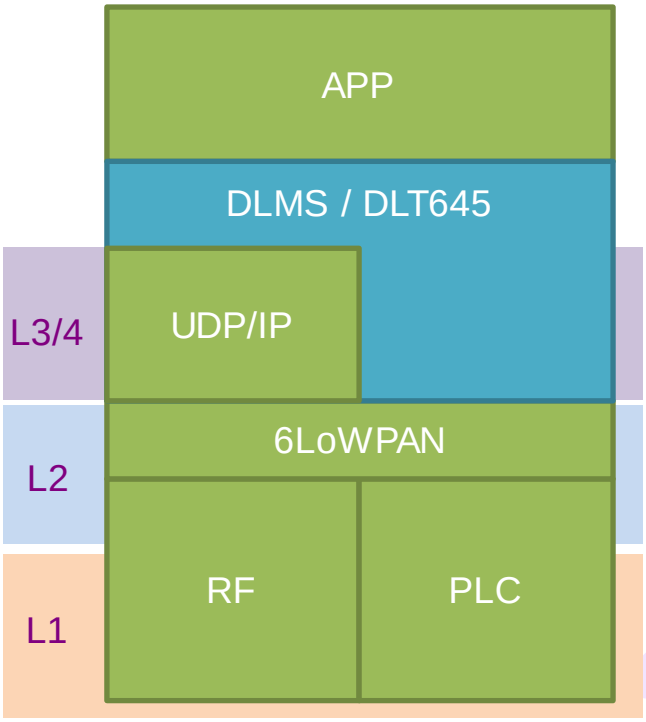


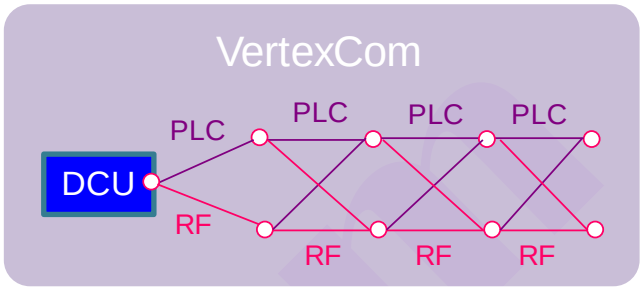
System Block Diagram

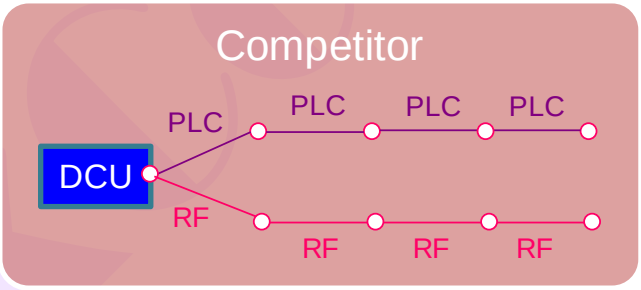
Figure 1. Smart Meter application example:



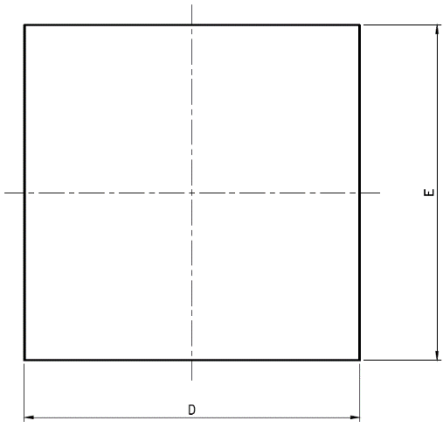
Dual Mode Software Feature

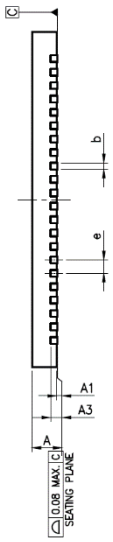


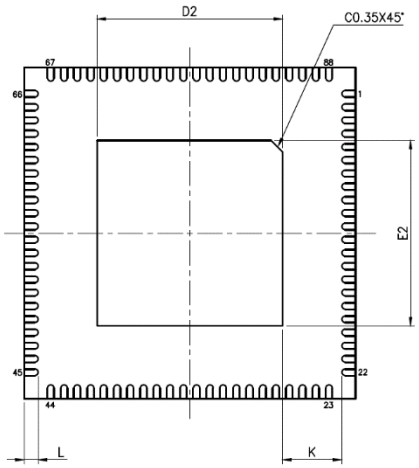




Package Information







	PACKAGE TYPE					
JEDEC OUTLINE	MO-220			MO-220		
PKG CODE	WQFN(XA88)			VQFN(YA88)		
SYMBOLS	MIN.	NOM.		MIN.	NOM.	MAX.
A	0.70	0.75	0.80	0.80	0.85	0.90
A1	0.00	0.02	0.05	0.00	0.02	0.05
A3	0.203 REF.			0.203 REF.		
D	10.00 BSC			10.00 BSC		
E	10.00 BSC			10.00 BSC		
e	0.40 BSC			0.40 BSC		
L	0.35	0.40	0.45	0.35	0.40	0.45
K	0.20	—	—	0.20	—	—

PAD SIZE	D2			E2			b			LEAD FINISH		JEDEC CODE
	MIN.	NOM.	MAX.	MIN.	NOM.	MAX.	MIN.	NOM.	MAX.	Pure Tin	PPF	
276X27* MIL	6.75	6.80	6.85	6.75	6.80	6.85	0.15	0.20	0.25	V	X	(W)VNNE-1

NOTES :

1. ALL DIMENSIONS ARE IN MILLIMETERS.
2. DIMENSION b APPLIES TO METALLIZED TERMINAL AND IS MEASURED BETWEEN 0.15mm AND 0.30mm FROM THE TERMINAL TIP. IF THE TERMINAL HAS THE OPTIONAL RADIUS ON THE OTHER END OF THE TERMINAL, THE DIMENSION b SHOULD NOT BE MEASURED IN THAT RADIUS AREA.
3. BILATERAL COPLANARITY ZONE APPLIES TO THE EXPOSED HEAT SINK SLUG AS WELL AS THE TERMINALS.

Ordering Information

Part No.	Description	Frequency Band	Standards	MCU	Flash	RAM	PKG	Body Size
VC8320U	Broadband PLC + RF Dual Mode SoC	1.9 - 12 MHz, SGCC HPLC 0.7 - 2.99 MHz	China SGCC Q/GDW 11612, IEEE 1901.1	ARM Cortex M4	2 MB	128 KB	QFN-88	10 x 10mm
VC8310GU	Narrowband PLC + RF Dual Mode SoC	0 - 500 KHz	G3-PLC, IEEE P1901.2, ITU-T G.hnem	ARM Cortex M4	2 MB	128 KB	QFN-88	10 x 10mm
VC8310PU	Narrowband PLC + RF Dual Mode SoC	0 - 500 KHz	PRIME v1.4 or v1.3.6	ARM Cortex M4	2 MB	128 KB	QFN-88	10 x 10mm