VertexCom

# VC6320

# Product Brief

**Version: 0.7**

**Release Date: Feb 1, 2019**

Specifications are subject to change without notice.

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# General Description

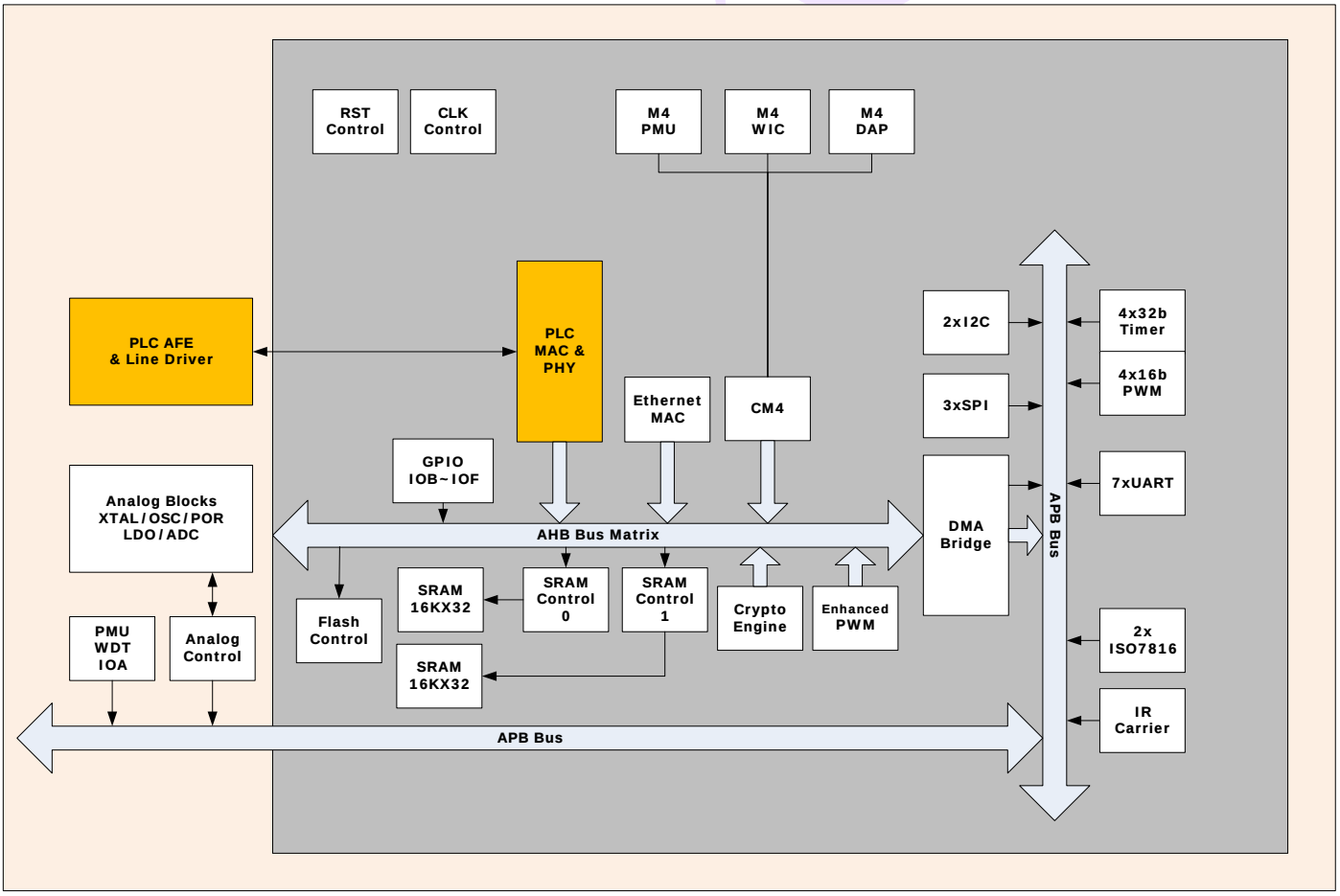
VC6320 is a broadband Power Line Communication (PLC) Processor. It integrates a 32-bit ARM Cortex M4 MCU and 32-bit DSP, embedded Flash memory, 7 UART interfaces, 3 SPI interfaces, 2 $I^2C$ interfaces, one 10/100M Ethernet MAC, PLC MAC/PHY layer functions, Analog-Front-End and high current Line Driver. VC6320 is a true single chip SoC that supports multiple modern broadband PLC standards for Smart Grid and other IIoT applications. VC6320 solution is optimized to provide the most robust AMI networking connectivity and state-of-the-art communication performance in the noisy electric grid environments.

# Features

- Support multiple Broadband PLC Standards: China SGCC Q/GDW 11612, IEEE 1901.1
- Support Frequency bands:
  - 1.9 MHz - 12 MHz
  - SGCC HPLC 0.7 MHz - 2.99 MHz
- Integrates high linearity, high current and power efficient Line Driver to offer the lowest BOM cost for Broadband PLC applications.
- Companion DC/DC buck converter VC6100 (Patented) for better power efficiency
- Support modulations: BPSK, QPSK and 16QAM
- Up to 7 UART interfaces
- Three SPI interfaces:
  - One SPI Master with 4 chip selects. It can be used to control wireless transceiver, metering or other SPI devices.
  - One SPI Slave interface for alternative data interface with Host Processor
  - 3rd SPI interface which can be configured as Master or Slave
- Two $I^2C$ interfaces
- Four 16-bit PWM timers
- One Ethernet MAC with RMII interface
- AES-128/192/256 and SM2/SM3/SM4 Crypto Accelerator
- 2 MB embedded Flash memory
- 128 KB SRAM

- Support In-System Programming of Flash memory via UART0 or SPI Slave interface
- Up to 53 programmable GPIOs for maximal flexibility
- 3.3V digital I/O
- Integrated DC/DC (3.3V to 1.2V) buck converter
- Chip power consumption:
  - TX Normal Mode: TBA mW
  - RX Listen Mode: TBA mW
  - Deep Sleep Mode: TBA mW
- Package:
  - 88L-QFN (10 x 10mm)
  - 60L-QFN (7 x 7mm)
- Operating temperature: -40 ~ +85°C
- Storage temperature: -40 ~ +125°C

# Functional Block Diagram



# System Block Diagram

**Figure 1.** Single-Phase PLC module application example:

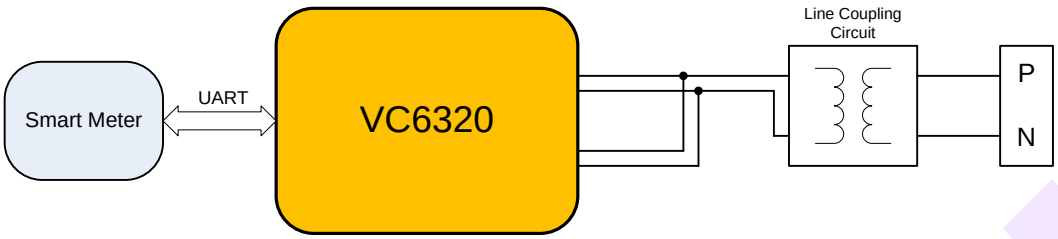
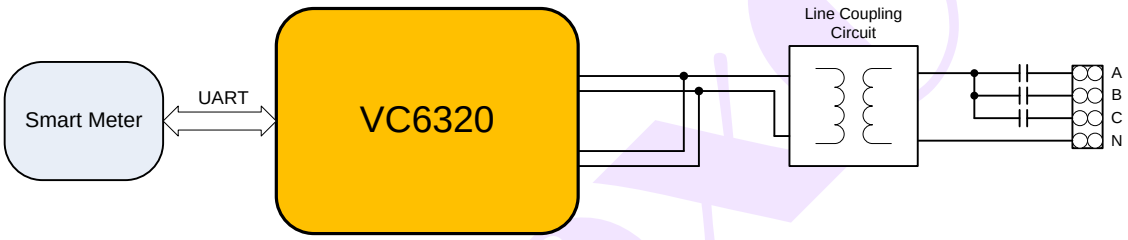



**Figure 2.** 3-Phase PLC module application example:

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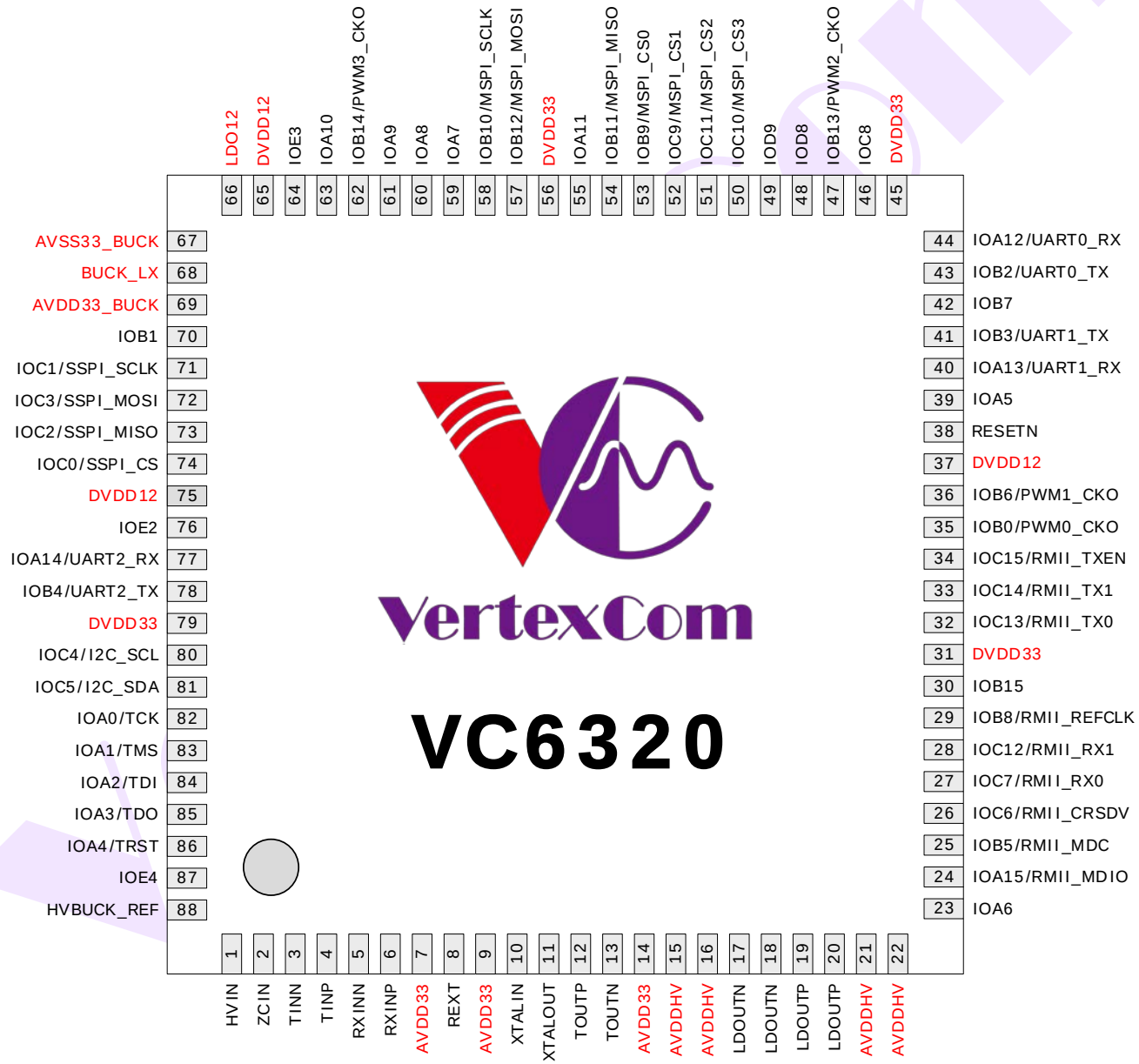
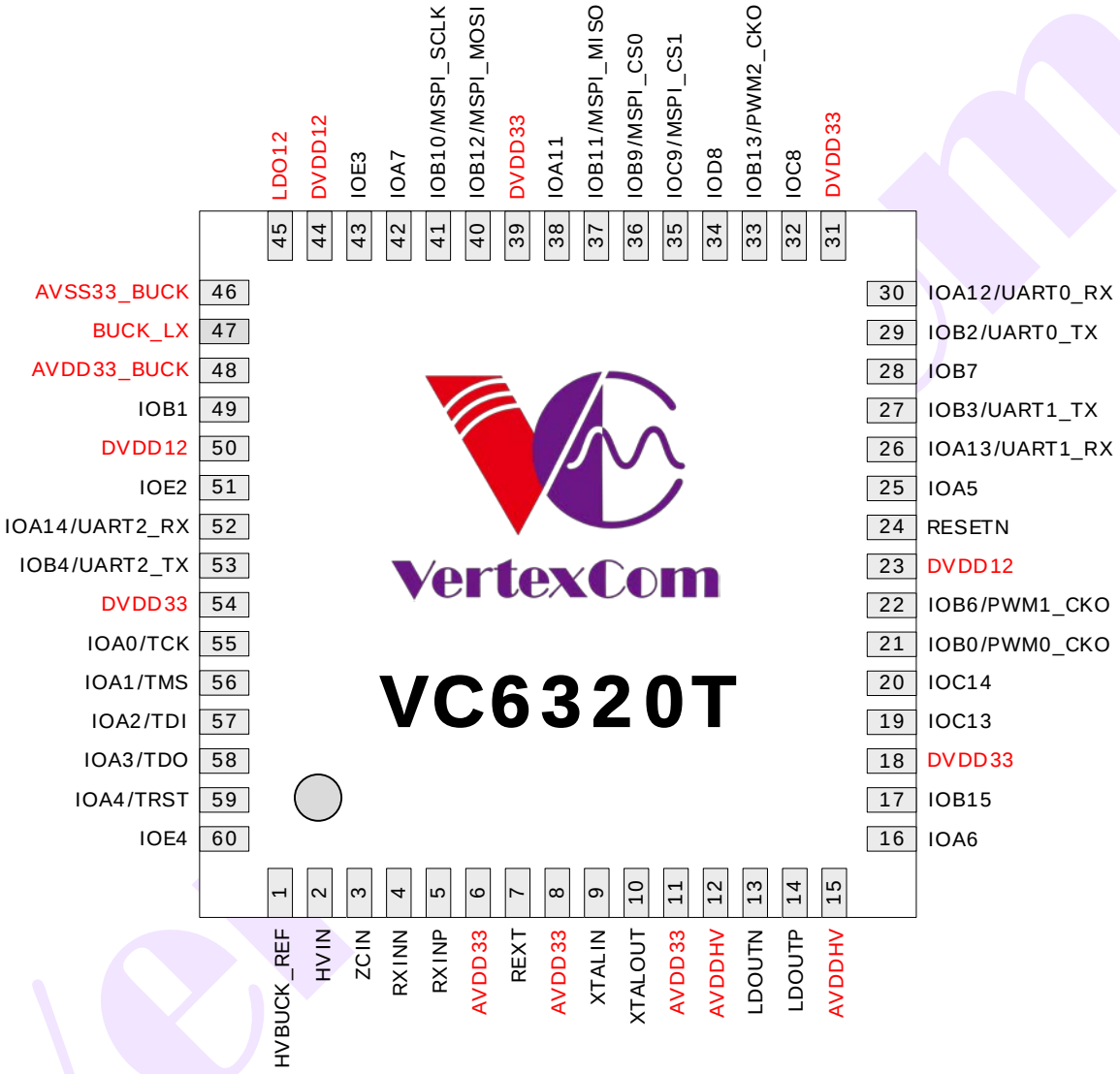
# Pin Assignments

## 88L-QFN



# 60L-QFN


LDO12 45
DVDD12 44
IOE3 43
IOA7 42
IOB10/MSPI_SCLK 41
IOB12/MSPI_MOSI 40
DVDD33 39
IOA11 38
IOB11/MSPI_MISO 37
IOB9/MSPI_CS0 36
IOC9/MSPI_CS1 35
IOD8 34
IOB13/PWM2_CKO 33
IOC8 32
DVDD33 31
AVSS33_BUCK 46
BUCK_LX 47
AVDD33_BUCK 48
IOB1 49
DVDD12 50
IOE2 51
IOA14/UART2_RX 52
IOB4/UART2_TX 53
DVDD33 54
IOA0/TCK 55
IOA1/TMS 56
IOA2/TDI 57
IOA3/TDO 58
IOA4/TRST 59
IOE4 60
30 IOA12/UART0_RX
29 IOB2/UART0_TX
28 IOB7
27 IOB3/UART1_TX
26 IOA13/UART1_RX
25 IOA5
24 RESETN
23 DVDD12
22 IOB6/PWM1_CKO
21 IOB0/PWM0_CKO
20 IOC14
19 IOC13
18 DVDD33
17 IOB15
16 IOA6
VertexCom
VC6320T
1 HVBUCK_REF
2 HVIN
3 ZCIN
4 RXINN
5 RXINP
6 AVDD33
7 REXT
8 AVDD33
9 XTALIN
10 XTALOUT
11 AVDD33
12 AVDDHV
13 LDOUTN
14 LDOUTP
15 AVDDHV

# Pin Descriptions

## 88L-QFN

(Pin type: “O”=Output, “I”= Input, “P”=Power, “G”=Ground)

| No. | Mnemonic | Type | Description |
|---|---|---|---|
| 1 | HVIN | I | High voltage measurement input. |
| 2 | ZCIN | I | Zero crossing detection input. |
| 3 | TINN | I | Input for engineering testing purpose. Keep floating or tie to ground. |
| 4 | TINP | I | Input for engineering testing purpose. Keep floating or tie to ground. |
| 5 | RXINN | I | Differential input (negative). |
| 6 | RXINP | I | Differential input (positive). |
| 7 | AVDD33 | P | Analog 3.3V power. |
| 8 | REXT | I | Connected to 60KOhm external resistor. |
| 9 | AVDD33 | P | Analog 3.3V power. |
| 10 | XTALIN | I | Input of Crystal oscillator driver. (25MHz) |
| 11 | XTALOUT | O | Output of Crystal oscillator driver. |
| 12 | TOUTP | O | Output for engineering testing purpose. Keep floating. |
| 13 | TOUTN | O | Output for engineering testing purpose. Keep floating. |
| 14 | AVDD33 | P | Analog 3.3V power. |
| 15 | AVDDHV | P | Analog 7V power. |
| 16 | AVDDHV | P | Analog 7V power. |
| 17 | LDOUTN | O | Line Driver differential output (negative). |
| 18 | LDOUTN | O | Line Driver differential output (negative). |

| No. | Mnemonic | Type | Description |
|---|---|---|---|
| 19 | LDOUTP | O | Line Driver differential output (positive). |
| 20 | LDOUTP | O | Line Driver differential output (positive). |
| 21 | AVDDHV | P | Analog 7V power. |
| 22 | AVDDHV | P | Analog 7V power. |
| 23 | IOA6 | I/O | General Purpose I/O. |
| 24 | IOA15<br>RMII_MDIO<br>UART3_RX | I/O<br>I/O<br>I | General Purpose I/O.<br>MDIO signal of RMII interface.<br>Data input of UART port 3. |
| 25 | IOB5<br>RMII_MDC<br>UART3_TX | I/O<br>O<br>O | General Purpose I/O.<br>MDC signal of RMII interface.<br>Data output of UART port 3. |
| 26 | IOC6<br>RMII_CRSDV | I/O<br>I | General Purpose I/O.<br>CRSDV signal of RMII interface. |
| 27 | IOC7<br>RMII_RX0 | I/O<br>I | General Purpose I/O.<br>RX data bit 0 of RMII interface. |
| 28 | IOC12<br>RMII_RX1 | I/O<br>I | General Purpose I/O.<br>RX data bit 1 of RMII interface. |
| 29 | IOB8<br>RMII_REFCLK<br>UART6_TX | I/O<br>I<br>O | General Purpose I/O.<br>50MHz reference clock input of RMII interface.<br>Data output of UART port 6. |
| 30 | IOB15<br>UART6_RX | I/O<br>I | General Purpose I/O.<br>Data input of UART port 6. |
| 31 | DVDD33 | P | Digital 3.3V power. |

| No. | Mnemonic | Type | Description |
|---|---|---|---|
| 32 | IOC13<br>RMII_TXD0 | I/O<br>O | General Purpose I/O.<br>TX data bit 0 of RMII interface. |
| 33 | IOC14<br>RMII_TXD1 | I/O<br>O | General Purpose I/O.<br>TX data bit 1 of RMII interface. |
| 34 | IOC15<br>RMII_TXEN | I/O<br>O | General Purpose I/O.<br>TXEN signal of RMII interface. |
| 35 | IOB0<br>PWM0_CKO<br>UART4_RX | I/O<br>O<br>I | General Purpose I/O.<br>PWM0 clock output.<br>Data input of UART port 4. |
| 36 | IOB6<br>PWM1_CKO<br>UART4_TX | I/O<br>O<br>O | General Purpose I/O.<br>PWM1 clock output.<br>Data output of UART port 4. |
| 37 | DVDD12 | P | Digital core power. |
| 38 | RESETN | I | Reset input (active low). |
| 39 | IOA5 | I/O | General Purpose I/O. |
| 40 | IOA13<br>UART1_RX | I/O<br>I | General Purpose I/O.<br>Data input of UART port 1. |
| 41 | IOB3<br>UART1_TX | I/O<br>O | General Purpose I/O.<br>Data output of UART port 1. |
| 42 | IOB7<br>UART5_TX | I/O<br>O | General Purpose I/O.<br>Data output of UART port 5. |
| 43 | IOB2<br>UART0_TX | I/O<br>O | General Purpose I/O.<br>Data output of UART port 0. |

| No. | Mnemonic | Type | Description |
|---|---|---|---|
| 44 | IOA12<br>UART0_RX | I/O<br>I | General Purpose I/O.<br>Data input of UART port 0. |
| 45 | DVDD33 | P | Digital 3.3V power. |
| 46 | IOC8 | I/O | General Purpose I/O. |
| 47 | IOB13<br>PWM2_CKO | I/O<br>O | General Purpose I/O.<br>PWM2 clock output. |
| 48 | IOD8 | I/O | General Purpose I/O. |
| 49 | IOD9 | I/O | General Purpose I/O. |
| 50 | IOC10<br>MSPI_CS3 | I/O<br>O | General Purpose I/O.<br>Master SPI chip select output 3. |
| 51 | IOC11<br>MSPI_CS2 | I/O<br>O | General Purpose I/O.<br>Master SPI chip select output 2. |
| 52 | IOC9<br>MSPI_CS1 | I/O<br>O | General Purpose I/O.<br>Master SPI chip select output 1. |
| 53 | IOB9<br>MSPI_CS0 | I/O<br>O | General Purpose I/O.<br>Master SPI chip select output 0. |
| 54 | IOB11<br>MSPI_MISO | I/O<br>I | General Purpose I/O.<br>Master SPI data input. |
| 55 | IOA11 | I/O | General Purpose I/O. |
| 56 | DVDD33 | P | Digital 3.3V power. |
| 57 | IOB12<br>MSPI_MOSI | I/O<br>O | General Purpose I/O.<br>Master SPI data output. |
| 58 | IOB10 | I/O | General Purpose I/O. |

| No. | Mnemonic | Type | Description |
|---|---|---|---|
| | MSPI_SCLK | O | Master SPI clock output. |
| 59 | IOA7 | I/O | General Purpose I/O. |
| 60 | IOA8 | I/O | General Purpose I/O. |
| 61 | IOA9 | I/O | General Purpose I/O. |
| 62 | IOB14<br>PWM3_CKO | I/O<br>O | General Purpose I/O.<br>PWM3 clock output. |
| 63 | IOA10 | I/O | General Purpose I/O. |
| 64 | IOE3 | I/O | General Purpose I/O. |
| 65 | DVDD12 | P | Digital core power. |
| 66 | LDO12 | P | Internal LDO core voltage power, connect 10uF to GND. |
| 67 | AVSS33_BUCK | G | Analog ground of switching regulator. |
| 68 | BUCK_LX | P | Power output of switching regulator. |
| 69 | AVDD33_BUCK | P | Analog 3.3V input of switching regulator. |
| 70 | IOB1<br>UART5_RX | I/O<br>I | General Purpose I/O.<br>Data input of UART port 5. |
| 71 | IOC1<br>SSPI_SCLK | I/O<br>I | General Purpose I/O.<br>Slave SPI clock input. |
| 72 | IOC3<br>SSPI_MOSI | I/O<br>I | General Purpose I/O.<br>Slave SPI data input. |
| 73 | IOC2<br>SSPI_MISO | I/O<br>O | General Purpose I/O.<br>Slave SPI data output. |
| 74 | IOC0 | I/O | General Purpose I/O. |

| No. | Mnemonic | Type | Description |
|---|---|---|---|
| | SSPI_CS | I | Slave SPI chip select input. |
| 75 | DVDD12 | P | Digital core power. |
| 76 | IOE2 | I/O | General Purpose I/O. |
| 77 | IOA14<br>UART2_RX | I/O<br>I | General Purpose I/O.<br>Data input of UART port 2. |
| 78 | IOB4<br>UART2_TX | I/O<br>O | General Purpose I/O.<br>Data output of UART port 2. |
| 79 | DVDD33 | P | Digital 3.3V power. |
| 80 | IOC4<br>I2C_SCL | I/O<br>O | General Purpose I/O.<br>I2C host port serial clock. |
| 81 | IOC5<br>I2C_SDA | I/O<br>I/O | General Purpose I/O.<br>I2C host port serial data. |
| 82 | IOA0 | I/O | General Purpose I/O. |
| 83 | IOA1 | I/O | General Purpose I/O. |
| 84 | IOA2 | I/O | General Purpose I/O. |
| 85 | IOA3 | I/O | General Purpose I/O. |
| 86 | IOA4 | I/O | General Purpose I/O. |
| 87 | IOE4 | I/O | General Purpose I/O. |
| 88 | HVBUCK_REF | O | Reference signal to high-voltage power regulator. |
| | EPAD | G | Must be tied to GND. |

# 60L-QFN

(Pin type: “O”=Output, “I”= Input, “P”=Power, “G”=Ground)

| No. | Mnemonic | Type | Description |
|---|---|---|---|
| 1 | HVBUCK_REF | O | Reference signal to high-voltage power regulator. |
| 2 | HVIN | I | High voltage measurement input. |
| 3 | ZCIN | I | Zero crossing detection input. |
| 4 | RXINN | I | Differential input (negative). |
| 5 | RXINP | I | Differential input (positive). |
| 6 | AVDD33 | P | Analog 3.3V power. |
| 7 | REXT | I | Connected to 60KOhm external resistor. |
| 8 | AVDD33 | P | Analog 3.3V power. |
| 9 | XTALIN | I | Input of Crystal oscillator driver. (25MHz) |
| 10 | XTALOUT | O | Output of Crystal oscillator driver. |
| 11 | AVDD33 | P | Analog 3.3V power. |
| 12 | AVDDHV | P | Analog 7V power. |
| 13 | LDOUTN | O | Line Driver differential output (negative). |
| 14 | LDOUTP | O | Line Driver differential output (positive). |
| 15 | AVDDHV | P | Analog 7V power. |
| 16 | IOA6 | I/O | General Purpose I/O. |
| 17 | IOB15<br>UART6_RX | I/O<br>I | General Purpose I/O.<br>Data input of UART port 6. |
| 18 | DVDD33 | P | Digital 3.3V power. |

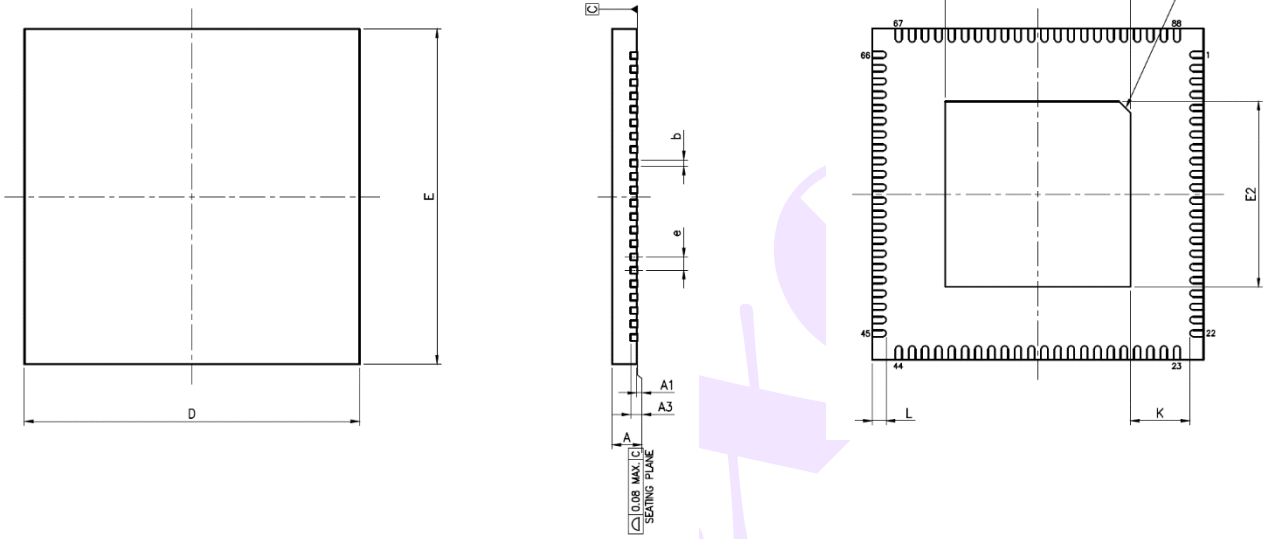
| No. | Mnemonic | Type | Description |
|---|---|---|---|
| 19 | IOC13<br>RMII_TXD0 | I/O<br>O | General Purpose I/O.<br>TX data bit 0 of RMII interface. |
| 20 | IOC14<br>RMII_TXD1 | I/O<br>O | General Purpose I/O.<br>TX data bit 1 of RMII interface. |
| 21 | IOB0<br>PWM0_CKO<br>UART4_RX | I/O<br>O<br>I | General Purpose I/O.<br>PWM0 clock output.<br>Data input of UART port 4. |
| 22 | IOB6<br>PWM1_CKO<br>UART4_TX | I/O<br>O<br>O | General Purpose I/O.<br>PWM1 clock output.<br>Data output of UART port 4. |
| 23 | DVDD12 | P | Digital core power. |
| 24 | RESETN | I | Reset input (active low). |
| 25 | IOA5 | I/O | General Purpose I/O. |
| 26 | IOA13<br>UART1_RX | I/O<br>I | General Purpose I/O.<br>Data input of UART port 1. |
| 27 | IOB3<br>UART1_TX | I/O<br>O | General Purpose I/O.<br>Data output of UART port 1. |
| 28 | IOB7<br>UART5_TX | I/O<br>O | General Purpose I/O.<br>Data output of UART port 5. |
| 29 | IOB2<br>UART0_TX | I/O<br>O | General Purpose I/O.<br>Data output of UART port 0. |
| 30 | IOA12<br>UART0_RX | I/O<br>I | General Purpose I/O.<br>Data input of UART port 0. |

| No. | Mnemonic | Type | Description |
|---|---|---|---|
| 31 | DVDD33 | P | Digital 3.3V power. |
| 32 | IOC8 | I/O | General Purpose I/O. |
| 33 | IOB13<br>PWM2_CKO | I/O<br>O | General Purpose I/O.<br>PWM2 clock output. |
| 34 | IOD8 | I/O | General Purpose I/O. |
| 35 | IOC9<br>MSPI_CS1 | I/O<br>O | General Purpose I/O.<br>Master SPI chip select output 1. |
| 36 | IOB9<br>MSPI_CS0 | I/O<br>O | General Purpose I/O.<br>Master SPI chip select output 0. |
| 37 | IOB11<br>MSPI_MISO | I/O<br>I | General Purpose I/O.<br>Master SPI data input. |
| 38 | IOA11 | I/O | General Purpose I/O. |
| 39 | DVDD33 | P | Digital 3.3V power. |
| 40 | IOB12<br>MSPI_MOSI | I/O<br>O | General Purpose I/O.<br>Master SPI data output. |
| 41 | IOB10<br>MSPI_SCLK | I/O<br>O | General Purpose I/O.<br>Master SPI clock output. |
| 42 | IOA7 | I/O | General Purpose I/O. |
| 43 | IOE3 | I/O | General Purpose I/O. |
| 44 | DVDD12 | P | Digital core power. |
| 45 | LDO12 | P | Internal LDO core voltage power, connect 10uF to GND. |
| 46 | AVSS33_BUCK | G | Analog ground of switching regulator. |

| No. | Mnemonic | Type | Description |
|---|---|---|---|
| 47 | BUCK_LX | P | Power output of switching regulator. |
| 48 | AVDD33_BUCK | P | Analog 3.3V input of switching regulator. |
| 49 | IOB1<br>UART5_RX | I/O<br>I | General Purpose I/O.<br>Data input of UART port 5. |
| 50 | DVDD12 | P | Digital core power. |
| 51 | IOE2 | I/O | General Purpose I/O. |
| 52 | IOA14<br>UART2_RX | I/O<br>I | General Purpose I/O.<br>Data input of UART port 2. |
| 53 | IOB4<br>UART2_TX | I/O<br>O | General Purpose I/O.<br>Data output of UART port 2. |
| 54 | DVDD33 | P | Digital 3.3V power. |
| 55 | IOA0 | I/O | General Purpose I/O. |
| 56 | IOA1 | I/O | General Purpose I/O. |
| 57 | IOA2 | I/O | General Purpose I/O. |
| 58 | IOA3 | I/O | General Purpose I/O. |
| 59 | IOA4 | I/O | General Purpose I/O. |
| 60 | IOE4 | I/O | General Purpose I/O. |
| | EPAD | G | Must be tied to GND. |

# Package Information

## 88L-QFN



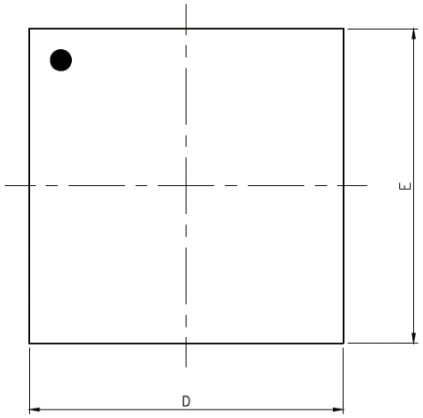

| | PACKAGE TYPE | | | | | |
|---|---|---|---|---|---|---|
| JEDEC OUTLINE | MO-220 | | | MO-220 | | |
| PKG CODE | WQFN(XA88) | | | VQFN(YA88) | | |
| SYMBOLS | MIN. | NOM. | | MIN. | NOM. | MAX. |
| A | 0.70 | 0.75 | 0.80 | 0.80 | 0.85 | 0.90 |
| A1 | 0.00 | 0.02 | 0.05 | 0.00 | 0.02 | 0.05 |
| A3 | 0.203 REF. | | | 0.203 REF. | | |
| D | 10.00 BSC | | | 10.00 BSC | | |
| E | 10.00 BSC | | | 10.00 BSC | | |
| e | 0.40 BSC | | | 0.40 BSC | | |
| L | 0.35 | 0.40 | 0.45 | 0.35 | 0.40 | 0.45 |
| K | 0.20 | — | — | 0.20 | — | — |

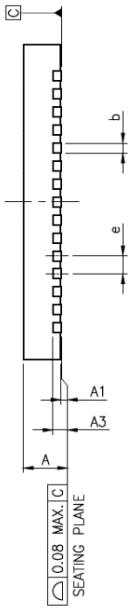
| PAD SIZE | D2 | | | E2 | | | b | | | LEAD FINISH | | JEDEC CODE |
|---|---|---|---|---|---|---|---|---|---|---|---|---|
| | MIN. | NOM. | MAX. | MIN. | NOM. | MAX. | MIN. | NOM. | MAX. | Pure Tin | PPF | |
| 276X27* MIL | 6.75 | 6.80 | 6.85 | 6.75 | 6.80 | 6.85 | 0.15 | 0.20 | 0.25 | V | X | (W)VNNE-1 |

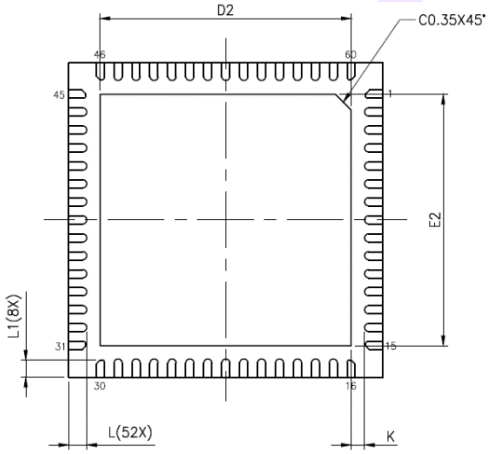
NOTES :

1. ALL DIMENSIONS ARE IN MILLIMETERS.
2. DIMENSION b APPLIES TO METALLIZED TERMINAL AND IS MEASURED BETWEEN 0.15mm AND 0.30mm FROM THE TERMINAL TIP. IF THE TERMINAL HAS THE OPTIONAL RADIUS ON THE OTHER END OF THE TERMINAL, THE DIMENSION b SHOULD NOT BE MEASURED IN THAT RADIUS AREA.
3. BILATERAL COPLANARITY ZONE APPLIES TO THE EXPOSED HEAT SINK SLUG AS WELL AS THE TERMINALS.

# 60L-QFN




PAD SIZE : 228X22* MIL

| | PACKAGE TYPE | | | | | |
|---|---|---|---|---|---|---|
| JEDEC OUTLINE | N/A | | | N/A | | |
| PKG CODE | WQFN(X760) | | | VQFN(Y760) | | |
| SYMBOLS | MIN. | NOM. | MAX. | MIN. | NOM. | MAX. |
| A | 0.70 | 0.75 | 0.80 | 0.80 | 0.85 | 0.90 |
| A1 | 0.00 | 0.02 | 0.05 | 0.00 | 0.02 | 0.05 |
| A3 | 0.203 REF. | | | 0.203 REF. | | |
| D | 6.90 | 7.00 | 7.10 | 6.90 | 7.00 | 7.10 |
| E | 6.90 | 7.00 | 7.10 | 6.90 | 7.00 | 7.10 |
| e | 0.40 BSC | | | 0.40 BSC | | |
| K | 0.20 | — | — | 0.20 | — | — |

NOTES :
1. ALL DIMENSIONS ARE IN MILLIMETERS.
2. DIMENSION b APPLIES TO METALLIZED TERMINAL AND IS MEASURED BETWEEN 0.15mm AND 0.30mm FROM THE TERMINAL TIP. IF THE TERMINAL HAS THE OPTIONAL RADIUS ON THE OTHER END OF THE TERMINAL, THE DIMENSION b SHOULD NOT BE MEASURED IN THAT RADIUS AREA.
3. BILATERAL COPLANARITY ZONE APPLIES TO THE EXPOSED HEAT SINK SLUG AS WELL AS THE TERMINALS.

| PAD SIZE | b | | | D2 | | | E2 | | | L1 | | | L | | | LEAD FINISH | | JEDEC CODE |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| | MIN. | NOM. | MAX. | MIN. | NOM. | MAX. | MIN. | NOM. | MAX. | MIN. | NOM. | MAX. | MIN. | NOM. | MAX. | Pure Tin | PPF | |
| ⚠2 228X22* MIL | 0.15 | 0.20 | 0.25 | 5.50 | 5.60 | 5.70 | 5.50 | 5.60 | 5.70 | 0.33 | 0.38 | 0.43 | 0.35 | 0.40 | 0.45 | V | X | N/A |

"*"表示汎用字元,此汎用字元可能被其它不同字元所取代,實際的字元請參照bonding diagram所示.
"*" is an universal character, which means maybe replaced by specific character, the actual character please refers to the bonding diagram.

# Ordering Information

| Part No. | Description | Frequency Band | Standards | MCU | Flash | RAM | PKG | Body Size |
|---|---|---|---|---|---|---|---|---|
| VC6320 | Broadband PLC SoC (QFN-88) w/Integrated Line Driver | 1.9 - 12 MHz<br>SGCC HPLC 0.7 - 2.99 MHz | China SGCC Q/GDW 11612, IEEE 1901.1 | ARM Cortex M4 | 2 MB | 128 KB | QFN-88 | 10 x 10mm |
| VC6320T | Broadband PLC SoC (QFN-60) w/Integrated Line Driver | 1.9 - 12 MHz<br>SGCC HPLC 0.7 - 2.99 MHz | China SGCC Q/GDW 11612, IEEE 1901.1 | ARM Cortex M4 | 2 MB | 128 KB | QFN-60 | 7 x 7mm |

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